# Test Results for a Didactic Chip Designed for Study of the Basic Analog CMOS Building Blocks

Gustavo da S. Ghedim, Patrick P. Domingues, Rodolfo V. de Almeida and Estêvão C. Teixeira
Engineering College
Federal University of Juiz de Fora – UFJF
Juiz de Fora – MG, Brazil
<gustavo.ghedim, patrick.protazio, rodolfo.almeida>@engenharia.ufjf.br, estevao.teixeira@ufjf.edu.br

***Abstract*— This work describes some test results for a didactic chip designed in order to improve the understanding of the basic analog CMOS building blocks. Free tools were used for schematics capture, simulation, layout editing, extraction and verification. The chip was fabricated on a 0.5-µm, standard CMOS process. It contains different types of current mirrors, a current adder, analog switches, differential pairs and basic amplifiers, which are briefly described.**

***Keywords*—Didactic chip; CMOS; analog building blocks; free EDA tools; test results**

## I. INTRODUCTION

The courses related to Analog Electronics (and their support bibliography) emphasizes currently the study of topologies well suited for integrated implementation, such as the polarization by current sources (realized by current mirrors) and use of differential pairs [1]. However, the laboratory realization of these structures is quite difficult and impractical, if discrete components are used. Because of this, a gap can be observed between the theoretical study of these blocks and their experimental verification.

A project described in [2] was proposed in order to allow the study of the basic building blocks of an analog CMOS integrated circuit (IC). Like other works reported in literature, as in [3-5], a didactic IC was designed with a variety of blocks, like current mirrors and differential pairs, with the goal to let the undergraduate or graduate students to bias, configure and test blocks by themselves, getting an appropriate insight about analog integrated circuits.

The design was developed at the Federal University of Juiz de Fora – UFJF, during an undergraduate scientific initiation project. An important fact is that free Electronic Design Automation (EDA) tools were used. Besides the cost issues, the motivation for the use of free apps was their faster learning curve and easier installation procedures, if compared to most of the commercial platforms. Moreover, these tools were better suited to the still reduced number of researchers involved in the area of Microelectronics in UFJF, currently in its initial stage.

After some adaptations, the project was sent for tapeout and fabricated on a standard CMOS technology. This paper presents the main test results for some of the blocks. The blocks were tested individually or in composite configurations, proving the versatility of the chip on allowing the elaboration of several practical activities regarding analog CMOS circuits.

This work is organized as follows: the building blocks are briefly described in Section II, while the test results for some of them are described in Section III. The main conclusions are presented in Section IV.

## II. DESCRIPTION OF THE BUILDING BLOCKS

The chip is composed by a set of basic building blocks of an analog CMOS IC, as follows: (i) current mirrors, based on *n*-channel MOSFETs – NMOS and *p*-channel MOSFETs – PMOS, in different topologies; (ii) a common source amplifier with active load; (iii) a source follower; (iv) a NMOS differential pair; (v) a PMOS differential pair (with cascodes); (vi) a current adder (NMOS); and (vii) analog switches (CMOS, NMOS and PMOS). Most of these structures are explained in [6].

### A. *Current mirrors*

There are sixteen NMOS mirrors, with different topologies and current ratings, and the same number of PMOS mirrors. All the mirrors have two outputs. Some of the basic mirrors were laid out intentionally unmatched, for comparison with their counterparts designed under well-known matching techniques.

In order to allocate a reasonable variety of blocks without exceeding the pin count of the chip, all the current mirrors of same type (NMOS or PMOS) share the same pins, by means of an analog multiplexer. This uses analog CMOS switches to convey the input/output currents into the selected mirror, as described in Fig. 1. The switches are selected by a 4-to-16 line decoder, which is the only one digital block of the chip.

The parameters of the mirrors are described in Table I. Each NMOS mirror of the table has a PMOS counterpart with same features.

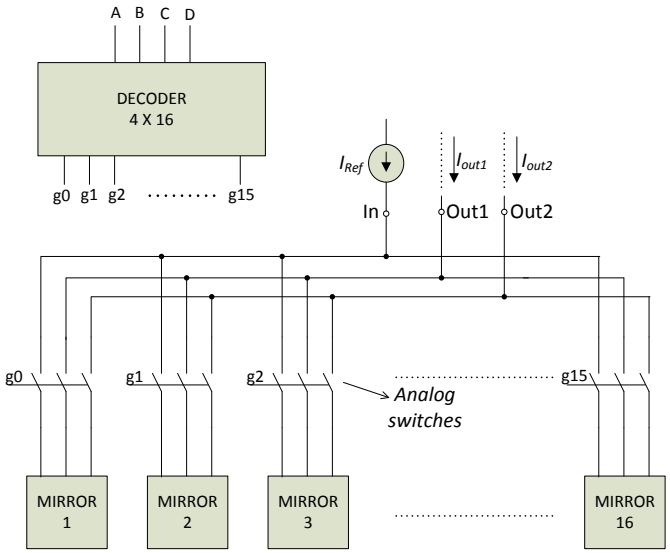



Fig. 1. Current mirrors mutiplexing scheme.

TABLE I. PARAMETERS OF THE CURRENT MIRRORS.

| Mirror No. | Parameters | | |
|---|---|---|---|
| | Topology | Rating (µA) | Matching |
| 1 | Basic | 40/40/40 | Matched |
| 2 | Basic | 40/40/40 | Unmatched |
| 3 | Basic | 40/80/80 | Matched |
| 4 | Basic | 40/80/80 | Unmatched |
| 5 | Basic | 80/80/80 | Matched |
| 6 | Basic | 80/80/80 | Unmatched |
| 7 | Basic | 80/160/160 | Matched |
| 8 | Basic | 80/160/160 | Unmatched |
| 9 | Wilson | 40/40/40 | All Matched |
| 10 | Cascode | 40/40/40 | |
| 11 | Cascode | 80/80/80 | |
| 12 | Cascode | 80/160/160 | |
| 13 | Modified Wilson | 40/40/40 | |
| 14 | Modified Wilson | 80/80/80 | |
| 15 | High compliance | 40/40/40 | |
| 16 | High compliance | 80/80/80 | |

### B. *Common-source amplifier and source follower*

A common-source (CS) amplifier with an active load, often referred as an analog inverter with active load [6], is used typically as the second stage of the classic Miller Operational Transconductance Amplifier (OTA), and has a high theoretical relevance. This block is included in order to be studied separately from any other. An independent source follower (SF) amplifier was also included.

### C. *Differential pairs*

The differential pair is a fundamental building block, since it is encountered at the first stage of any OTA or operational amplifier. Two differential pairs were designed: a simple NMOS differential pair and a PMOS differential pair with cascode.

### D. *Current adders*

The NMOS current adder is a combination of two cascode mirrors. The cascode configuration can give high output impedance. With this structure, it is possible to plan several practices emphasizing the current-mode analog processing.

### E. *Analog switches*

There are four analog switches: NMOS, PMOS and two CMOS. The switches are controlled by the first four output lines of the 4-to-16 decoder.

### F. *Die features*

The chip was fabricated in the ON Semi C5N Process (5 V, 0.5-µm, NWELL, triple metal, standard CMOS), with an area of approx. 3.81 mm$^2$ (1.95 mm x 1.95 mm). The used package is a DIP40 (40 pins). The Fig. 2 shows the die microphotograph, with identification of its main blocks. The structures called "general analog blocks" contain the CS, the SF and the differential pairs.

## III. TEST RESULTS

The chip contains a reasonable quantity of blocks to be tested. In order to perform this task, a development board was developed. The board contains passive components, as resistors, trimpots and capacitors. It also contains configuration switches and pins for monitoring of the signals.

The test results for some blocks will be presented. If necessary, the peripheral circuit needed to configure a block will also be shown, to give a better comprehension of the result described.

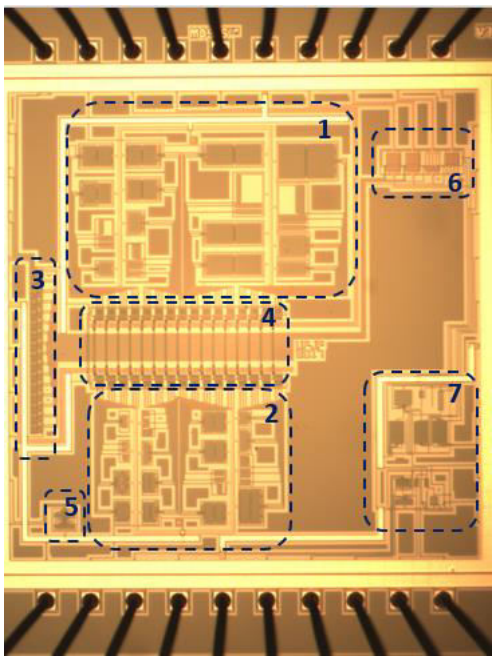



Fig. 2. Die microphotograph, with identification of its main blocks: 1 – PMOS mirrors; 2 – NMOS mirrors; 3 – 4-to-16 line decoder; 4 – analog switches of the mirrors multiplexers; 5 – NMOS current adder; 6 – general purpose analog switches; 7 – general analog blocks.

### A. *Current mirrors*

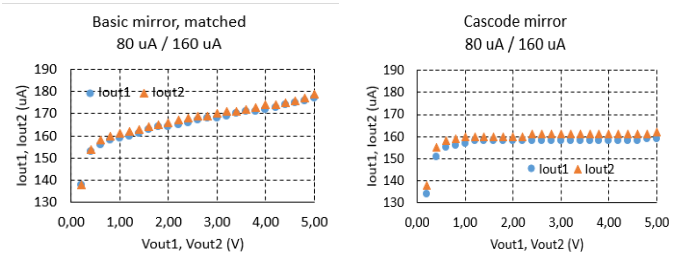
The current mirrors were biased with their nominal input currents, and for the output currents their $I_{OUT}$ *x* $V_{OUT}$ characteristics were evaluated. The Fig. 3a shows the output currents plots for the Mirror No. 7 (Basic, 80 µA input, 160 µA outputs – see the Table I), and Fig. 3b shows the plots for the Mirror No. 12 (Cascode, 80 µA input, 160 µA outputs). It can be seen that for a cascode configuration, there is a little variation of $I_{OUT}$ with $V_{OUT}$ (considering the transistors in saturation), due to the high output impedance of this topology.

### B. *Current adder*

The ability to sum two currents flowing into the inputs of the current adder could be tested by fixing one of the currents at 40 µA (the nominal value) and varying the other current within the range of 25 to 80 µA. The results for 24 different measurements are expressed in Fig. 4, and prove the capability of the structure in summing two current signals.

### C. *Common source amplifier*

The setup for the CS amplifier is shown in Fig. 5. The amplifier was biased with 40 µA (current biasing circuit not shown). Using a decoupling capacitor ($C_1$), a small AC signal was applied to the gate of MOSFET $M_1$, superimposed to a DC bias voltage set by resistors $R_{1\_1}$ and $R_{1\_2}$. The resistor $R_{load}$ in parallel with capacitor $C_{load}$ represents the oscilloscope probe used to measure the output signal.




(a) (b)

Fig. 3. Experimental $I_{OUT}$ *x* $V_{OUT}$ plots for two current mirrors: (a) basic (matched), 80 µA/160 µA; (b) cascode, 80 µA/160 µA.

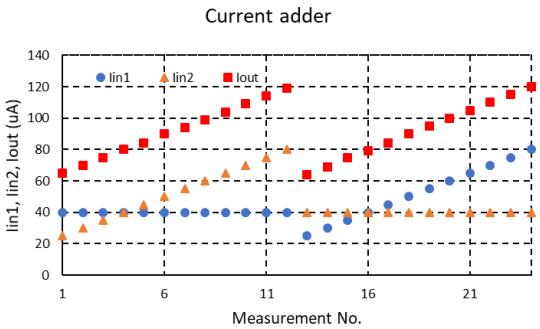



Fig. 4. Measurements for the current adder. In the figure, there are shown the input currents ($I_{IN1}$ and $I_{IN2}$) and the output current ($I_{OUT}$).

An input signal with 20 mV(pp) and frequency 1 kHz was applied, resulting in an output voltage with 2.64 V(pp). This corresponds to a gain of 42.4 dB. The acquired waveforms for the input and output signals are shown in Fig. 6. It is possible to verify the phase inverting between the input and the output signal, what justifies the terminology "analog inverter" for this configuration.

### D. *Source follower*

The network for biasing the SF amplifier is similar to that used in the CS amplifier, as can be seen in Fig. 7. The circuit was also biased with 40 µA.

However, since the source follower does not provide voltage amplification, but current (or charge) amplification, it usually handles AC signals with greater magnitudes, in practice pre-amplified by a previous stage, like a CS amplifier, for example.

Therefore, the test was performed by applying an AC input signal with amplitude 2.04 V(pp), 10 kHz. The gate voltage on $M_2$ (AC+DC component) and the output voltage are shown in Fig. 8. The magnitude of the output signal was of 1.76 V(pp), resulting in a gain of 0.86 (-1.28 dB). In fact, the SF gives a gain slightly lower than unity, with no phase inversion between the input and output signals, as can be seen in the figure.

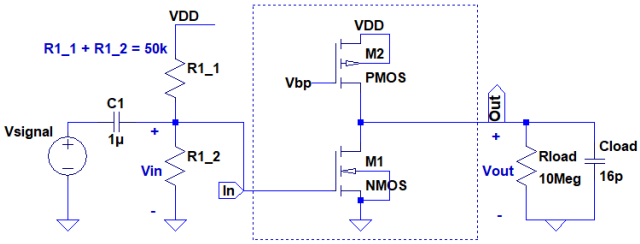



Fig. 5. Setup for testing the CS amplifier. The on-chip elements are surrounded by the dashed line.

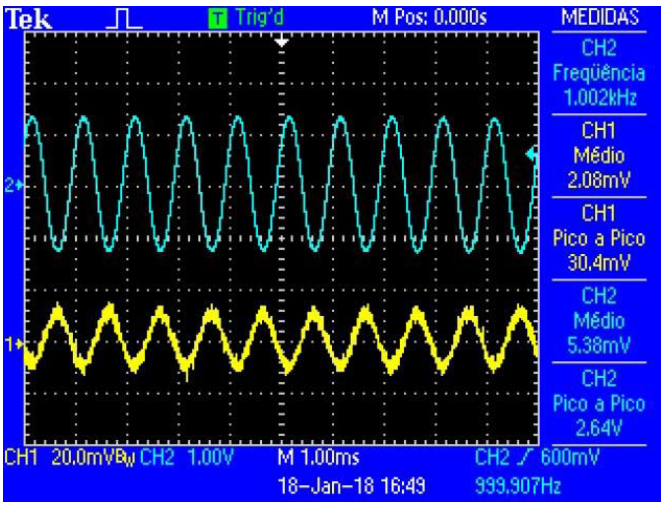



Fig. 6. Signals obtained for the CS amplifier. : Channel 1: AC input signal (20 mV/div.); Channel 2: output signal (1 V/div.). Horizontal: 1 ms/div.

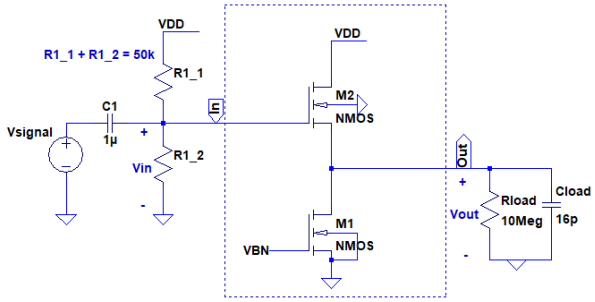



Fig. 7. Setup for testing the SF amplifier.

## IV. Conclusions

This paper described the test results achieved for a chip designed for the study of the basic building blocks of the analog CMOS circuits. The objective of the project is to shorten the existing gap between the theory and practice regarding the fundamentals of analog integrated circuits.

Due to the paper size restriction, a limited number of experimental results were shown in this work. However, all the blocks mentioned in Section II were tested, with results consistent with the theoretical analysis and the simulation results obtained previously.

By using the development board specially designed for the chip, a great variety of practices can be organized, allowing the experimentation of the blocks individually or in composite assemblings. For example, the output of a CS amplifier can be connected to the input of a SF amplifier, resulting in a cascaded amplifier with both voltage and current gains.

The practical activities can be developed by undergraduate or even graduate students. The elaboration of a manual with proposal of practices can be considered as a future work.

## Acknowledgments

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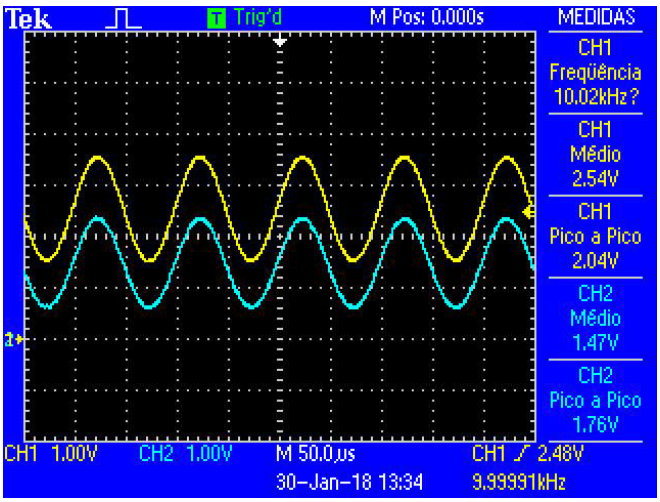


Fig. 8. Signals obtained for the SF amplifier. : Channel 1: signal at the gate of $M_2$ (1 V/div.); Channel 2: output signal (1 V/div.). Horizontal: 50 µs/div.

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